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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LIN, KENNY S	
ART UNIT	PAPER NUMBER
2152	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/068,157	HALLENBECK, PETER D.	
	Examiner	Art Unit	
	Kenny Lin	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-15 and 57-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-15 and 57-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 7-15 and 57-77 are presented for examination. Claims 1-6 and 16-56 are canceled.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 7-15 and 57-68, 70, 72, 74 and 76 are rejected under 35 U.S.C. 102(b) as being anticipated by Dolin Jr. et al (Dolin), US 5,737,529.

4. Dolin was cited in the IDS by the applicant.

5. As per claim 7, Dolin taught the invention as claimed including a machine readable memory encoded with a data structure for aliasing inputs to provide a single virtual input in a premises automation system, the data structure comprising:

a. A description of a logical relationship (col.11, lines 59-67, col.12, lines 1-23, table I, II, III, IX, XI);

b. A plurality of entries related to a premises to which entries the logical relationship applies, each entry producing a Boolean result on which the logical relationship

operates to produce a single Boolean outcome for the single virtual input (col.9, lines 59-67, table I, II, V, IX, XI), each entry further comprising:

i. At least a first input identifier serving as a first operand (col.11, lines 59-67, col.12, lines 1-23, table I, II; e.g. temp_in);

ii. At least one operator (col.11, lines 59-67, col.12, lines 1-23, table I, II; e.g. when); and

iii. At least a second operand (col.11, lines 59-67, col.12, lines 1-23, table I, II; e.g. io_changes(temp_in)); and

Wherein a storage bit corresponds to the single virtual input to represent status information of the premises wherein the status information cannot be represented by a single physical input (col.9, lines 59-67, col.12, lines 44-46, table V).

6. As per claim 11, Dolin taught the invention as claimed including a method for aliasing inputs in a premises automation system, the method comprising:

a. Producing a plurality of Boolean results, one Boolean result for each of a plurality of entries related to a premises, each entry further comprising at least a first input identifier serving as a first operand, at least one operator, and at least a second operand (col.6, lines 48-67, col.7, lines 1-17, col.9, lines 59-67, col.11, lines 59-67, col.12, lines 1-23, table I, II, III, V, IX, XI);

b. Applying a logical relationship to the plurality of Boolean results to produce a single Boolean outcome for a single virtual input (col.6, lines 65-67, col.7, lines

1-2, col.9, lines 59-67, col.11, lines 59-67, col.12, lines 1-23, table I, II, III, V, IX, XI); and

c. Setting a storage bit corresponding the single virtual input to represent status information of the premises wherein the status information cannot be represented by a single physical input (col.9, lines 59-67, col.12, lines 44-46, table V).

7. As per claim 15, Dolin taught the invention as claimed including apparatus for providing a single virtual input in a premises automation system, the apparatus comprising:

a. Means for producing a plurality of Boolean results, one Boolean result for each of a plurality of entries related to a premises, each entry further comprising at least a first input identifier serving as a first operand, at least one operator, and at least a second operand (col.11, lines 59-67, col.12, lines 1-23, table I, II, III, V, IX, XI);

b. Means for applying a logical relationship to the plurality of Boolean results to produce a single Boolean outcome for the single virtual input (col.6, lines 65-67, col.7, lines 1-2, col.9, lines 59-67, col.11, lines 59-67, col.12, lines 1-23, table I, II, III, V, IX, XI); and

c. Means for setting a storage bit corresponding to the single virtual input to represent status information of the premises wherein the status information cannot be represented by a single physical input (col.9, lines 59-67, col.12, lines 44-46, table V).

8. As per claim 57, Dolin taught the invention as claimed including an input/output unit for use in premises automation, the input/output unit comprising:

a. A processor for controlling the operation of the I/O unit (col.6, lines 48-56; control cells; col.10, lines 43-63);

b. A plurality of inputs operatively connected to the processor, at least some of the inputs operable receive communication related to a premises from premises-based apparatus (col.6, lines 48-67, col.7, lines 1-2, col.10, lines 43-63, table V); and

c. A memory connected to the processor, the memory encoded with program code to enable the processor to control the operation of the I/O unit to provide input aliasing through a data structure (col.10, lines 43-63) further comprising:

i. A description of a logical relationship (col.11, lines 59-67, col.12, lines 1-23, tables I, II, III, V, IX, XI);

ii. A plurality of entries corresponding to the inputs to which entries the logical relationship applies, each entry producing a Boolean result on which the logical relationship operates to produce a single Boolean outcome for a single virtual input (col.6, lines 65-67, col.7, lines 1-2, col.9, lines 59-67, table I, II, V, IX, XI), each entry further comprising:

1. at least a first input identifier serving as a first operand (col.11, lines 59-67, col.12, lines 1-23, table I, II, V);

2. at least one operator (col.11, lines 59-67, col.12, lines 1-23, table I, II, V); and

3. at least a second operand (col.11, lines 59-67, col.12, lines 1-23, table I, II, V);

wherein a storage bit corresponding to the virtual input represents status information of the premises wherein the status information cannot be represented by a single physical input (col.9, lines 59-67, col.12, lines 44-46, table V).

9. As per claim 61, Dolin taught the invention as claimed including an input/output unit for use in premises automation, the input/output unit comprising:

a. A processor for controlling the operation of the I/O unit (col.6, lines 48-56; control cells; col.10, lines 43-63);

b. A plurality of inputs operatively connected to the processor, at least some of the inputs operable to receive communication related to a premises from premises-based apparatus (col.6, lines 48-67, col.7, lines 1-2, col.10, lines 43-63); and

c. A memory connected to the processor, the memory encoded with program code to enable the processor to control the operation of the I/O unit to provide input aliasing by producing a plurality of Boolean results (col.10, lines 43-63), one Boolean result for each of a plurality of entries, each entry further comprising at least a first input identifier and applying a logical relationship to the plurality of Boolean results to produce a single Boolean outcome for setting a storage bit as a single virtual input representing status information of the premises wherein the status information cannot be represented by a single physical input (col.6, lines

65-67, col.7, lines 1-2, col.9, lines 59-67, col.11, lines 59-67, col.12, lines 1-23, 44-46, table I, II, III, V, IX, XI).

10. As per claims 8 and 12, 58, 62, Dolin taught the invention as claimed in claims 7, 11, 57, 61. Dolin further taught that the second operand in the least one of the plurality of entries is a second input identifier (col.11, lines 59-67, col.12, lines 1-23).

11. As per claims 9-10 and 13-14, 59-60, 63-64, Dolin taught the invention as claimed in claims 7-8, 11-12, 57-58, 61-62. Dolin further taught that the second operand in at least one of the plurality of entries is a stored value (col.11, lines 59-67, col.12, lines 1-23).

12. As per claim 65, Dolin taught the invention as claimed in claim 15. Dolin further taught that the second operand in at least one of the plurality of entries is a data structure including a second input identifier (col.11, lines 59-67, col.12, lines 1-23).

13. As per claims 66-67, Dolin taught the invention as claimed in claims 15 and 65. Dolin further taught that the second operand in at least one of the plurality of entries is a data structure including a stored value (col.11, lines 59-67, col.12, lines 1-23).

14. As per claims 68, 70, 72, 74 and 76, Dolin taught the invention as claimed in claims 7, 11, 15, 57 and 61. Dolin further taught that the first input identifier is formatted so that the first

input identifier alone can specify any of a plurality of distributed inputs in the premises automation system (table I, input bit temp_in).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 69, 71, 73, 75 and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dolin Jr. et al (Dolin), US 5,737,529.

17. As per claims 69, 71, 73, 75 and 77, Dolin taught the invention as claimed in claims 68, 70, 72, 74 and 76. Dolin further taught that the first input identifier is further formatted to include an input number (table I, input bit temp_in). Dolin did not specifically teach the first input identifier to include a unit number. However, Dolin taught in other input identifiers to include unit numbers to control different temperature sensors (Table IV: sensor_1; sensor_2; sensor_3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Dolin and include unit numbers in the first input identifier in the temperature sensor control program to identifier different input temperature for different location and control temperature accordingly.

Response to Arguments

18. Applicant's arguments filed 12/6/2006 have been fully considered but they are not persuasive.

19. In the remark, applicant argued that (1) Dolin's tem0perature sensor is represented by a single physical input and thus the idea of reading and evaluating the status of a temperature sensor is exactly the opposite of, and teaches away from the invention which handles status information that cannot be represented by a single physical input. (2) The limitation of a plurality of data entries related to the premises producing a plurality of Boolean results, which are then combined is not shown in Dolin. (3) A term in applicant's claims cannot mean whatever the examiner wants it to mean, the term must mean what it is defined to mean in applicant's specification. The unit number identifies a hardware platform, not sensor numbers.

20. Examiner traverse the argument:

As to points (1), Dolin taught a logical relationship that produces a single virtual input in table V to turn on or off the motor using the program language of:

```
        Void motor (Boolean on_off_flag) {...}
and
        void control_action()
        {
        if ( AmOnline            ** Boolean variable
            Building Cooling     ** Boolean variable
            MinOffTimer  == 0
            OutletWaterTemp > OutletWater.HighSet
            CndnsrHeadTemp < CndnsrHead.LowSet
            CmprssrGasPrssr < CmprssrInltGas.LowSet
            CoolAirTemp > CoolAir.HighCet
          )
```

```
        {
                motor(on);
        }
        else {... motor(off); }
}
```

These logical relationship produces a single Boolean outcome by using the Boolean variable of on_off_flag to represent the status of the motor as on or off. The status of the motor is also represented by multiple inputs such as OutletWaterTemp, CndnsrHeadTemp, CmprssrGasPrssr and CoolAirTemp including two Boolean variables AmOnline and BuildingCooling. The **if** condition clearly shows that this relationship is a logical relationship.

As to point (2), Dolin taught to produce Boolean result for each temperature sensor to determine high temperature or not (e.g. temp_high=true or false) and applies these Boolean results to produce a single Boolean outcome to turn the fans on or off (col.6, lines 65-67, col.7, lines 1-2).

As to point (3), applicant's specification failed to define that the unit number identifies a *hardware platform* since the unit also be a software module. In addition, Dolin taught to use identifiers to identify hardware platforms such as temperature sensors (see Table IV: sensor_1; sensor_2; sensor_3). These sensor identifiers are used for identifying the sensors and directing controls thereto. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Dolin and include unit numbers in the first input identifier in the temperature sensor control program to identifier different input temperature for different location and control temperature accordingly.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenny Lin whose telephone number is (571) 272-3968. The examiner can normally be reached on 8 AM to 5 PM Tue.-Fri. and every other Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on (571) 272-3913. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ksl
February 8, 2007

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER